REMARKS

Claims 1-14 are all the claims pending in the application. By this Amendment, Applicant editorially amends claims 1, 2, 3, 6, 9, 11, and 14. The amendments to claims 1, 2, 3, 6, 9, 11, and 14 were made for reasons of precision of language and consistency, and do not narrow the literal scope of the claims and thus do not implicate an estoppel in the application of the doctrine of equivalents. The amendments to claims 1, 2, 3, 6, 9, 11, and 14 were not made for reasons of patentability.

In addition, by this Amendment, Applicant adds claims 15-18. Claims 15-18 are clearly supported throughout the specification *e.g.*, Fig. 1 and pages 3-5 of the specification.

Preliminary Matters

As preliminary matters, Applicant thanks the Examiner for returning the initialed form PTO/SB/08 submitted with the Information Disclosure Statement filed on November 2, 2005.

The Examiner failed to acknowledge the claim for priority under 35 U.S.C. §119(e), as well as the receipt of a certified copy of the priority document. Therefore, Applicant respectfully requests the Examiner to check the appropriate boxes on the Form PTO-326 indicating that the claim for priority is acknowledge and that the certified copy of the priority document has been received.

Moreover, the Examiner failed to acknowledge that the drawings are accepted. Therefore, Applicant respectfully requests the Examiner to check the appropriate box on the Form PTO-326 indicating that the drawings are accepted.

Summary of the Office Action

Claims 1-3, 9-11 and 14 are rejected under 35 U.S.C. § 102(b) and claims 4-7, 10 and 12-13 are rejected under 35 U.S.C. § 103(a).

Claim Rejection under 35 U.S.C. § 102

Claims 1-3, 9-11 and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,335,223 to Iino (hereinafter "Iino"). Applicant respectfully traverses these grounds of rejection in view of the following comments.

This response initially focuses on claim 1. Independent claim 1, among a number of unique features, recites: "phase correcting means for adjusting the phase reference identifier allocated to a respective data packet by a predetermined phase correcting value, leading in the phase, which corresponds to a maximum expected delay for a transfer of the data packets on the first transfer path or the second transfer path; and buffer means for buffering the data packets by buffering times such that for each respective data packet, buffering time and delay needed for passing through the network device, in total correspond to the maximum expected delay taken into account in allocated, adjusted phase reference identifier of respective data packet."

In the conventional techniques, it is disclosed that related packets of a frame could pass through different transfer paths within the device and redundant data packets will pass on different transfer path from the original data packets. When the transfer paths vary in length, a delay is caused and the data packets passed in different paths are no longer in the same phase relationship to one another at the output stage of the network device.

In an exemplary, non-limiting embodiment, it is disclosed that a frame contains phase reference identifier for determining a respective position of the data packet within the

corresponding frame. Accordingly, the network device has a pointer processor that adjusts the phase reference identifier by a predetermined correcting value, leading in phase. That is, the phase reference identifier is adjusted to correspond to a maximum possible delay for transfer of the data packets in various transfer paths. A delay may actually be smaller. Accordingly, buffers are provided to obtain the total needed delay (maximum possible delay - worst case scenario). It will be appreciated that the foregoing remarks relate to the invention in a general sense, the remarks are not necessarily limitative of any claims and are intended only to help the Examiner better understand the distinguishing aspects of the claims mentioned above.

The Examiner alleges that claim 1 is directed to a network device and is anticipated by Iino. Specifically, the Examiner alleges that a frame former 10 along with a frame comparator 33 disclose the adjusting means as set forth in claim 1 and that buffer 61 discloses a buffering means as set forth in claim 1 (*see* pages 2-3 of the Office Action). Applicant has carefully studied Iino's discussion of a pointer processing circuit and Applicant respectfully submits that Iino fails to disclose or suggest adjusting a pointer so that it leads in phase and corresponds to a maximum expected propagation delay and fails to disclose or suggest the buffer buffering the packet so that the buffering time and the delay to pass through the network device correspond to the maximum expected delay.

Iito discloses that the cross connect equipment receives multiplexed input frame signals from one input side transmission line and, at the same time, receives the multiplexed input frame signals from other input side transmission lines. The received frame signals need phase adjustment (col. 1, line 33 to col. 2, line 3). Accordingly, a pointer processing circuit in a

SONET system, which can easily process the pointer values of the transmission frame signals passing through the cross connect equipment even in a case where transmission frame signals are supplied from a plurality of input side transmission lines, is provided (co. 2, lines 5 to 12). The pointer processing circuit is installed in the reception part of the cross connect equipment to process the signals prior to the cross connection, thereby simplifying the phase adjustment (col. 2, lines 13 to 22).

Specifically, Iito discloses a frame counter 10 generating timing signals for reconstructing the transport overhead region such as A1, A2 ... H1, H2, J1 ... and so on. The pointers H1 and H2 represent the distance or number of time slots from a byte H3 (stuff byte used to fill in the shortage of the data bytes, col. 4, lines 3 to 12) to the byte J1 (a signal indicative of a position from the pointer dropping unit indicated the head position of the data frame, col. 3, lines 14 to 16 and col. 4, lines 21 to 30). Iito discloses a pointer comparing unit 9 receiving both the reception side byte J1 given from the pointer dropping unit 3 and the transmission side byte J1' given from the frame counter 10 so that the phase difference between the two is produced therefrom. The information of the phase difference is supplied to the pointer inserting units 5-1 and 5-2. At the pointer inserting units 5-1 and 5-2, the position of the byte J1 in the data region of the input frame signal is modified to become the transmission byte J1' in the data region of the output frame signal, according to the aforesaid information of the phase difference (Fig. 4, col. 5, lines 12 to 28).

In Iito, however, it is only disclosed that the frame counter 10 has a 1/N divider 71, a 1/8 divider 72, a 1/90 divider 73, a 1/9 divider 74 and a decoder 75, to produce respective byte

positions of the transport overhead bytes. The 1/N divider 71, where N is a positive integer, divides the basic clock N*51.84 MHz (Fig. 10; col. 9, lines 17 to 30) and that the frame comparator 33 compares byte J1 given from the pointer dropping unit 3 and the transmission side byte J1' given from the frame counter 10 so that the phase difference between the two is output and produced. Iito fails to disclose or suggest the adjusting the pointer by a phase correcting value that leads in phase and that corresponds to a maximum expected delay. That is, in Iito, the delay of the previous packet (value J1') occurring on the transmission side is used to adjust the phase of the received signal. Iito fails to disclose or suggest using a maximum expected delay to adjust phase of the incoming signal.

Moreover, the Examiner alleges that buffer 61 inherently accounts for the time for the signals needed to pass through the network device (*see* page 3 of the Office Action). Applicant respectfully submits that under the doctrine of "inherency," if an element is not expressly disclosed in a prior art reference, the reference will still be deemed to anticipate a subsequent claim if the missing element "is necessarily present in the thing described in the reference" *Cont'l Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991). "Inherent anticipation requires that the missing descriptive material is '**necessarily present,' not merely probably or possibly present**, in the prior art." (emphasis added) *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295, 63 U.S.P.Q.2d 1597, 1599 (Fed. Cir. 2002); see also MPEP §2112.

Iito discloses the buffer 61, which stores the input frame signal when a write payload clock is received. The write payload clock is extracted from the input frame signal. The frame

signal stored in the buffer 61 is read out from the buffer 61 when a read payload clock derived from the basic clock generated in the related transmission apparatus is received. The frame signal from the buffer 61 is input to the cross connect equipment 4 via an AND gate 62 and an OR gate 63 (Fig. 9; col. 8, lines 49 to 64). However, Iito fails to disclose or suggest that the buffering time will correspond to the maximum expected delay minus the time needed for passing through the network device. In other words, Iito does not explicitly or implicitly disclose that the buffering time is somehow related to the maximum delay.

Therefore, "phase correcting means for adjusting the phase reference identifier allocated to a respective data packet by a predetermined phase correcting value, leading in the phase, which corresponds to a maximum expected delay for a transfer of the data packets on the first transfer path or the second transfer path; and buffer means for buffering the data packets by buffering times such that for each respective data packet, buffering time and delay needed for passing through the network device, in total correspond to the maximum expected delay taken into account in allocated, adjusted phase reference identifier of respective data packet," as set forth in claim 1 is not disclosed by Iito, which lacks adjusting the phase reference identifier so that it corresponds to the maximum expected delay for transferring packets within the device and which lacks buffering the frame signals for a period of time that corresponds to maximum expected delay minus the actual time for propagating through the network device.

For at least these exemplary reasons, claim 1 patentably distinguishes (and is patentable over) Iito. Claims 2, 3, 8, and 9 are patentable at least by virtue of their dependency on claim 1.

In addition, claim 3 recites: "the maximum expected delay is substantially determined based on maximum lengths of connecting leads used for at least one of the first transfer path and the second transfer path." The Examiner alleges that maximum expected delay must be equal to the different phase in order to allow the signals to pass from input to output stage and thus inherently disclose the unique features cited above (*see* page 3 of the Office Action). Applicant respectfully submits that this ground of rejection is technically inaccurate.

That is, Iito discloses correcting actual delay, phase difference, based on the previously transmitted signal (*i.e.*, comparing J' (at the transmission side) with J (at the input side)). In other words, Iito fails to disclose or suggest a maximum expected delay. Moreover, Iito is silent with respect to the lengths of the leads of the transfer paths. In Iito, the leads of the paths could be of the same lengths (*see e.g.*, col. 1, lines 32 to 42, there is no problem with a cross connect equipment (having a number of paths) when there is a single input line). That is, different lengths of the transfer paths are not necessarily present in Iito. If the transfer paths are of equal length, they will not impact the delay and will not be a consideration in adjusting phase difference. Accordingly, Iito fails to disclose explicitly or implicitly the unique features of claim 3. For at least these additional reasons, claim 3 patentably distinguishes from Iito.

Next, independent claims 11 and 14 recite features similar to, although not necessarily coextensive with, the features argued above with respect to claim 1. Therefore, arguments presented with respect to claim 1 are respectfully submitted to apply with equal force here. For at least substantially analogous exemplary reasons, therefore, independent claims 11 and 14 are patentably distinguishable from Iito.

Claim Rejections under 35 U.S.C. § 103

Claims 4-7, 10, and 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iino. Applicant respectfully traverses these grounds for rejection in view of the following comments.

Claims 4-7, and 10 depend on claim 1 and claims 12 and 13 depend on claim 11. Applicant has already demonstrated that Iito does not meet all the requirements of independent claims 1 and 11. Accordingly, claims 4-7, 10, 12, and 13 are patentable at least by virtue of their dependency on claims 1 and 11.

In addition, the Examiner takes Official Notices that the features of claims 4-7, 10, 12, and 13 are well known (*see* pages 4-5 of the Office Action). These Official Notices are being traversed.

MPEP § 2144.03 recites: "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." Ordinarily, there must be some form of evidence in the record to support an assertion of common knowledge. See *Lee*, 277 F.3d at 1344-45, 61 USPQ2d at 1434-35 (Fed. Cir. 2002); *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697 (holding that general conclusions concerning what is "basic knowledge" or "common sense" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings, will not support an obviousness rejection), *also see* MPEP § 2144.03(B).

In the present case, the Examiner's personal reasoning in view of the Iito reference is not concrete evidence. Specifically, the Examiner alleges that having a redundant device and

redundant transfer paths, multiple switching matrixes, and so on are well known (*see* pages 4-5 of the Office Action). It is respectfully noted that various network devices have various elements but the Examiner's reasoning tends to suggest that if the various elements are individually known in the art then the network device is well known. However, it is the combination of various elements and their respective functions that creates the claimed network devices. By way of an example, it does not mean that because a wire is known, its placement anywhere within the network device is also well known. Applicant respectfully submits that the combination of elements forms the device as claimed and the Examiner is respectfully requested to provide references for the unique features set forth in the dependent claims.

Since Applicant is traversing the Examiner's assertions of Official Notice, the Examiner must provide documentary evidence in the next Office Action if the rejection is to be maintained. *Id.*

New Claims

In order to provide more varied protection, Applicant adds claims 15-18. Claim 15 is patentable at least by virtue of its recitation: "each of the first and second matrix units comprises: a pointer processor adjusting the phase reference identifier...,and a buffer buffering the data packets, where each data packet is buffered for a buffering time that corresponds to the maximum expected delay minus time needed to pass respective data packet through a respective transfer path." Iito discloses that adjustments can be simplified when the pointers are adjusted before the cross connect, as opposed to after the cross connect (col. 2, lines 13 to 22).

Accordingly, Iito fails to disclose or suggest each stage having a pointer processor that can adjust the phase reference identifier.

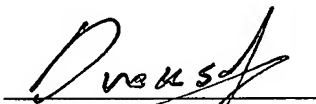
Claims 16-18 are patentable at least by virtue of their dependency on claim 15.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: March 7, 2006

Attorney Docket No.: Q67427